



## UM6116-V Series

### WIDE VOLTAGE 2K × 8 CMOS SRAM

#### Features

- Single +3 volt power supply
- Wide operating voltage range: 2.6 to 5.5V
- Current: Operating: 50 mA (max.)  
Standby: 1  $\mu$ A (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Pin compatible with standard 16K EPROM/Mask ROM
- Available in 24 pin DIP, SOP, and Skinny DIP packages or in Chip Form (See ordering information)

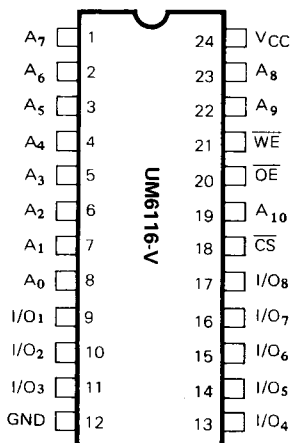
#### General Description

The UM6116-V is a 16,384-bit static random access memory organized as 2,048 words by 8 bits and operates on a wide operating voltage range. It is built with UMC's high performance CMOS process. Six-transistor full CMOS

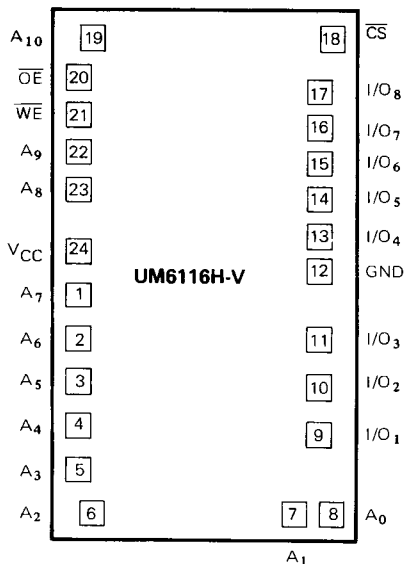
memory cell provides low standby current and high reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

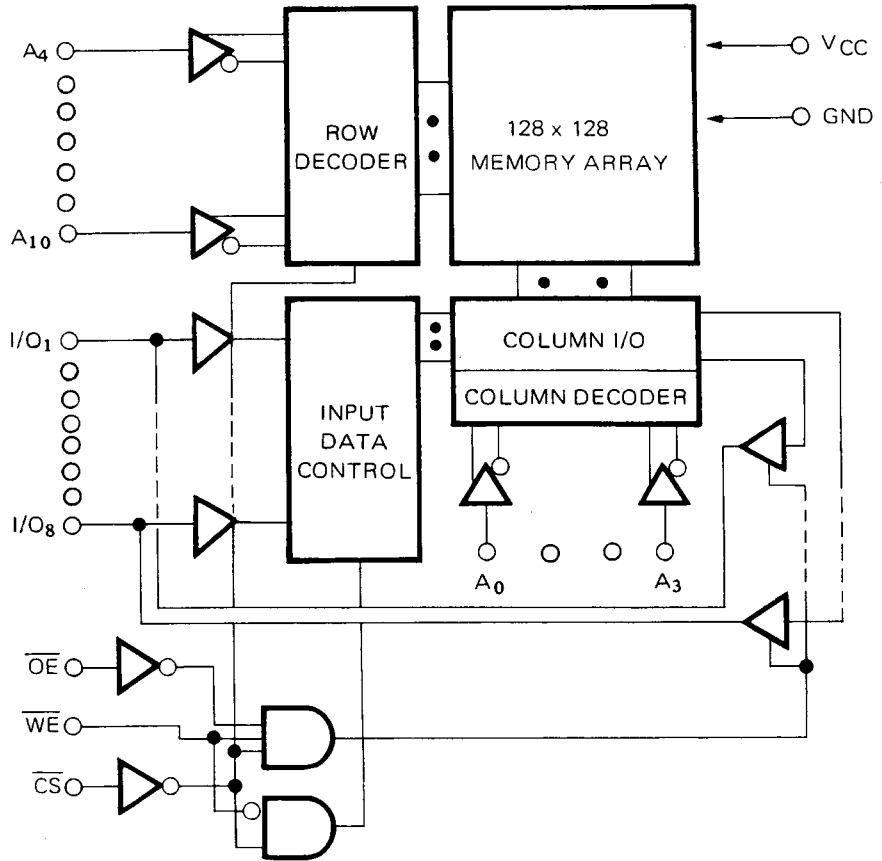
Standard  
SRAM

#### Pin Configuration



#### Pad Configuration



**Block Diagram**


**Pin Description**

Designation	Description
A <sub>0</sub> – A <sub>10</sub>	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O <sub>1</sub> – I/O <sub>8</sub>	Data Input/Output
V <sub>CC</sub>	Power Supply (+3V)
GND	Ground

**Recommended DC Operating Conditions**

 (T<sub>A</sub> = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.6	3.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> – 1.0	–	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input Low Voltage	–0.3	0	+0.8	V
C <sub>L</sub>	Output Load	–	–	100	pF
TTL	Output Load	–	–	1	–

**Absolute Maximum Ratings \***

V<sub>CC</sub> to GND . . . . . –0.5V to +7.0V  
 IN, IN/OUT Voltage to GND . . . . . –0.5V to V<sub>CC</sub> +0.3V  
 Operating Temperature, T<sub>opr</sub> . . . . . 0°C to +70°C  
 Storage Temperature, T<sub>stg</sub> . . . . . –55°C to +125°C  
 Temperature Under Bias, T<sub>bias</sub> . . . . . –10°C to +85°C  
 Power Dissipation, P<sub>T</sub> . . . . . 1.0W/SOP 0.7W  
 Soldering Temp. & Time . . . . . 260°C, 10 sec

**\*Comments**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 2.6V to 5.5V, GND = 0V)

Symbol	Parameter	UM6116-V		Unit	Test Conditions
		Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	–	1	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current	–	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ , or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>
I <sub>CC</sub>	Active Power Supply Current	–	50	mA	$\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA
I <sub>CC1</sub>	Dynamic Operating Current	–	50	mA	Min. Cycle, Duty = 100%, $\overline{CS} = V_{IL}$ I <sub>I/O</sub> = 0 mA
I <sub>SB</sub>	Standby Power Supply Current	–	1	mA	$\overline{CS} = V_{IH}$
I <sub>SB1</sub>		–	1	μA	$\overline{CS} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2V or V <sub>IN</sub> ≤ 0.2V
V <sub>OL</sub>	Output Low Voltage	–	0.2	V	I <sub>OL</sub> = 200 μA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> – 0.2	–	V	I <sub>OH</sub> = –100 μA

**Truth Table**

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	$V_{CC}$ Current
Standby	H	X	X	High Z	$I_{SB}, I_{SB1}$
Output Disabled	L	H	H	High Z	$I_{CC}, I_{CC1}$
Read	L	L	H	$D_{OUT}$	$I_{CC}, I_{CC1}$
Write	L	X	L	$D_{IN}$	$I_{CC}, I_{CC1}$

Note: X : H or L

**Capacitance**

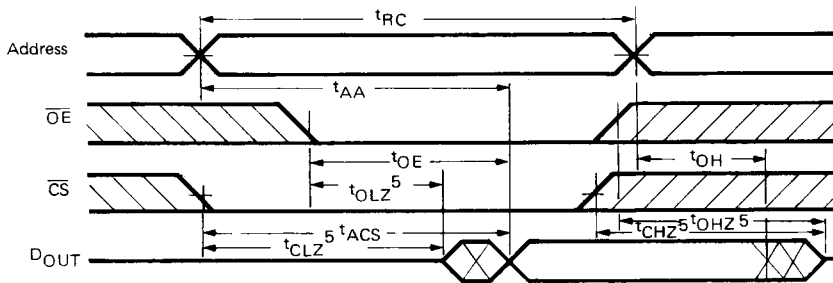
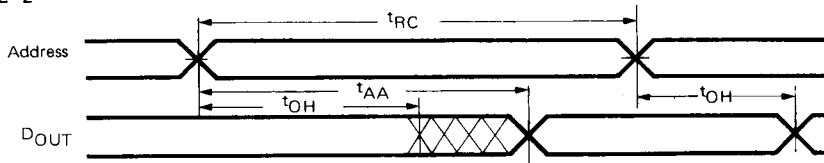
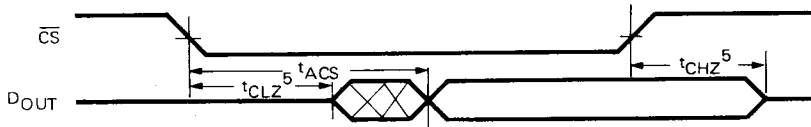
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
$C_{IN}^*$	Input Capacitance		6	pF	$V_{IN} = 0V$
$C_{I/O}^*$	Input/Output Capacitance		8	pF	$V_{I/O} = 0V$

\*This parameter is sampled and not 100% tested.

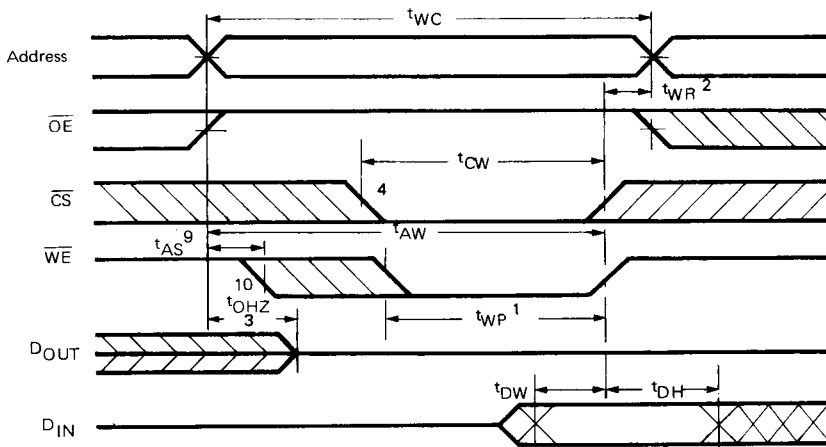
**AC Characteristics** ( $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 2.6V$  to  $5.5V$ ,  $GND = 0V$ )

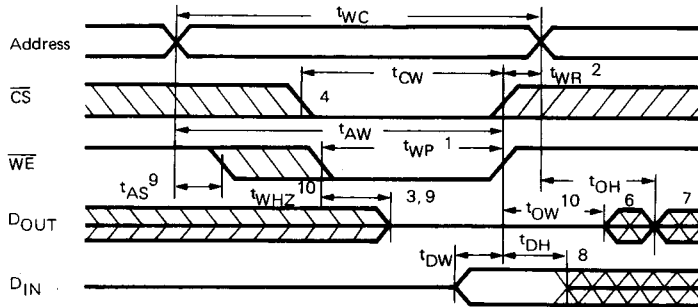
Symbol	Parameter	UM6116-V		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	1,000	—	ns
$t_{AA}$	Address Access Time	—	1,000	ns
$t_{ACS}$	Chip Select Access Time	—	1,000	ns
$t_{OE}$	Output Enable to Output Valid	—	200	ns
$t_{CLZ}$	Chip Selection to Output in Low Z	20	—	ns
$t_{OLZ}$	Output Enable to Output in Low Z	20	—	ns
$t_{CHZ}$	Chip Deselection to Output in High Z	—	200	ns
$t_{OHZ}$	Chip Disable to Output in High Z	—	200	ns
$t_{OH}$	Output Hold from Address Change	20	—	ns
<b>Write Cycle</b>				
$t_{WC}$	Write Cycle Time	1,000	—	ns
$t_{CW}$	Chip Selection to End of Write	500	—	ns
$t_{AS}$	Address Set-Up Time	10	—	ns
$t_{AW}$	Address Valid to End of Write	100	—	ns
$t_{WP}$	Write Pulse Width	500	—	ns
$t_{WR}$	Write Recovery Time	100	—	ns
$t_{WHZ}$	Write to Output in High Z	10	200	ns
$t_{DW}$	Data to Write Time Overlap	400	—	ns
$t_{DH}$	Data Hold from Write Time	50	—	ns
$t_{OHZ}$	Output Disable to Output in High Z	10	200	ns
$t_{OW}$	Output Active from End of Write	10	—	ns

Notes:  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve open circuit condition and are not referred to output voltage levels

**Timing Waveforms**
**READ CYCLE 1 (1)**

**READ CYCLE 2 (1,2,4)**

**READ CYCLE 3 (1,3,4)**

**Notes:**

1.  $\overline{WE}$  is High for Read Cycle.
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

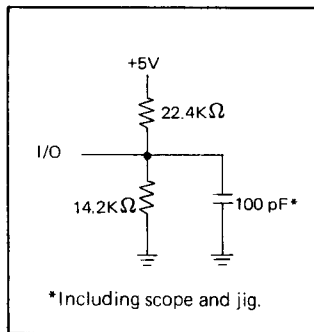
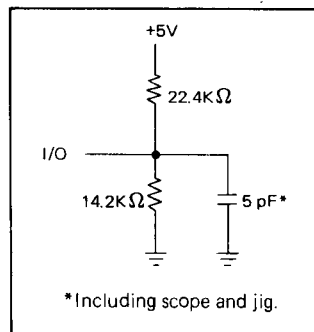
**WRITE CYCLE 1**


**WRITE CYCLE 2 (5)**

**Notes:**

1. A write occurs during the overlap (t<sub>WP</sub>) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
2. t<sub>WR</sub> is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
3. During this period, I/O pins are in the output state so the input signals of opposite phase to the outputs must not be applied.
4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
5.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
6. D<sub>OUT</sub> is the same phase of write data of this write cycle.
7. D<sub>OUT</sub> is the read data of next address.
8. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. t<sub>AS</sub> is measured from address valid to the beginning of write.
10. Transition is measured  $\pm 500$  mV from steady state. This parameter is sampled and not 100% tested.

**AC Test Conditions**

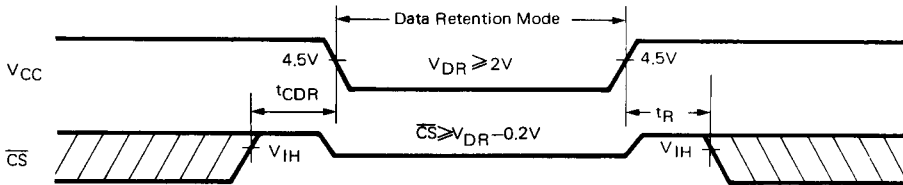
Input Pulse Levels	0.4V to $V_{CC} - 0.5V$
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	$V_{IL} = 0.5V$ , $V_{IH} = V_{CC} - 1.0V$ $V_{OL} = 0.2V$ , $V_{OH} = V_{CC} - 0.4V$
Output Load	See Fig. 1, 2


**Figure 1. Output Load**

**Figure 2. Output Load for t<sub>CLZ</sub>,  
t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>WHZ</sub>,  
and t<sub>OW</sub>**

**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
$V_{DR}$	$V_{CC}$ for Data Retention	2.0	—	V	$\overline{CS} \geq V_{CC} - 0.2V$
$I_{CCDR}$	Data Retention Current	—	1	$\mu\text{A}$	$V_{CC} = 3.0V, \overline{CS} \geq 2.8V$
$t_{CDR}$	Chip Deselect to Data Retention Time	0	—	ns	See Retention
$t_R$	Operation Recovery Time	$t_{RC}^*$	—	ns	Waveform

\* $t_{RC}$  = Read Cycle Time

**Timing Waveform Low  $V_{CC}$  Data Retention Waveform**

**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6116-V	1,000 ns	50	0.001	24L DIP
UM6116M-V	1,000 ns	50	0.001	24L SOP
UM6116K-V	1,000 ns	50	0.001	24L Skinny DIP
UM6116H-V	1,000 ns	50	0.001	Chip Form